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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/708,490	11/09/2000	Chie Iwasa	03180.0269	1827

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
1300 I STREET, NW
WASHINGTON, DC 20005

EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/708,490	IWASA, CHIE	
	Examiner	Art Unit	
	Tung S Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

a. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vu et al. (6,140,832) in view of Edmond et al. (U.S. Patent 5,381,103).

Regarding claim 1:

Vu discloses a semiconductor testing apparatus for testing semiconductor devices comprising a read circuit configured to read measurement data including a test vector data and data of good samples and data of faulty samples returned to a manufacturer (col. 2, lines 1-26); a determination circuit configured to supply the test vector data to the good samples and the faulty samples (col. 1, lines 40-51), and to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices; and an IDDQ measuring circuit configured to test semiconductor devices by applying the effective test vector (col. 1, lines 52-67).

Regarding claim 5:

Vu discloses a semiconductor testing method for testing semiconductor devices, comprising reading measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector (col. 1, lines 5-8, col. 1, lines 40-51), including a test vector data and data of good samples and faulty samples returned to a manufacturer; supplying the test vectors to the good samples and the faulty samples (col. 1,lines 52-67); determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices (col. 2, lines 1-25); and applying test vectors of the effective address pairs to the semiconductor devices for testing (col. 2, lines 1-25).

Regarding claim 9:

Vu discloses a program with which a semiconductor testing method for testing semiconductor devices is executed by a computer in a semiconductor testing apparatus which comprises a read circuit (col. 1, lines 5-20), a determination circuit (fig. 1), and an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector (abstract), the program comprising: instructions configured to read measurement data including a test vector data and data of good samples and faulty samples returned to a manufacturer (col.1, lines 40-67); instructions configured to supply the test vector data to good samples and faulty samples (col. 2, lines 1-25); instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices (col. 2, lines 1-25); and instructions configured to apply test vectors of the effective address pairs for testing (col. 2, lines 1-25).

Regarding claim 13:

Vu discloses a semiconductor testing method of specifying a faulty part in a semiconductor device, comprising: reading measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector (col. 1, lines 40-67), wherein the measurement data includes a test program (fig. 1), test vector data (fig. 3), data of good samples and faulty samples returned to a manufacturer (col. 2, lines 1-25); supplying test vector data to good and faulty samples (col. 2, lines 1-25); determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process; a applying test vectors of the effective address pairs to a semiconductor device (col. 2, lines 1-25, col. 3, lines 44-55); specifying a faulty part within the semiconductor device by measuring an emission from the semiconductor device (col. 2, lines 1-25).

Regarding claim 16:

Vu discloses a semiconductor testing apparatus for specifying a faulty part in a semiconductor device, comprising: a read circuit configured to read measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector (col. 1, lines 40-67), wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer (col. 2, lines 1-25); a determination circuit configured to supply the test vector data to the good

samples and faulty samples, and to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process (col. 2, lines 1-25); and a faulty part specifying circuit configured to apply test vectors of the effective address pairs to a semiconductor device and to specify a faulty part by measuring an emission from the semiconductor device (col. 2, lines 1-25, fig. 3).

Regarding claim 19:

Vu discloses a program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, the program comprising instructions configured to read measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector (col. 1, lines 40-67), wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer; instructions configured to supply the test vector data to good samples and faulty samples (col. 2, lines 1-25); instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process (col.2, lines 1-25); instructions to apply test vectors of the effective address pairs to a semiconductor device (col. 3, lines 44-55, fig. 4); and instructions to specify a faulty part within the semiconductor device by measuring an emission from the semiconductor device (col. 2, lines 1-25).

Regarding claims 2, 3, 4, 6, 7, 8, 10, 11, 12, 14, 15, 17 and 18:

Vu discloses a semiconductor testing method, program, apparatus for specifying a faulty part in a semiconductor device, including the rate of change in current value of the device (fig. 4), acquire effective address pair (fig. 4, col. 3, lines 44-55), display rate falling outside of the range of pass/fail decision criteria (col. 2, lines 1-25), measure current value for pass fail comparison (col. 2, lines 1-25), displaying result (fig. 2, 3, 4).

Vu does not disclose the sample returned by the user; Edmond discloses the sample returned by the user in order to have a good performance products (Col. 1, Lines 10-21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Vu to have the sample returned by the user taught by Edmond in order in order to have a good performance products (Col. 1, Lines 10-21).

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 703-305-3309. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone

numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TC2800 FAX Telephone Numbers: 703-872-9306

TC2800 Customer Service FAX - (703) 872-9317

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